What is claimed is:

1. A nonvolatile semiconductor memory device including a plurality of digit lines to which a plurality of nonvolatile memory cells are connected, wherein upon reading of memory cell information, the digit lines contain a first digit line connected to selected one of the nonvolatile memory cells; and a second digit line connected to only non-selected nonvolatile memory cells, while the memory cell information is read out with the first and second digit lines as a pair.

2. A nonvolatile semiconductor memory device as claimed in claim 1, wherein the first digit line and the second digit line adjoin each other.

3. A nonvolatile semiconductor memory device as claimed in claim 1, wherein the first digit line and the second digit line have equivalent physical parameters surrounding the first and second digit lines.

4. A nonvolatile semiconductor memory device as claimed in claim 1, further comprising a plurality of sectors, each of the sectors including a predetermined number of the nonvolatile memory cells and serving as a basic unit for accessing the nonvolatile memory cell, wherein

a positional relationship of the first digit line and the second digit line is inverted by each of the sector.

5. A nonvolatile semiconductor memory device as claimed in claim 1, further comprising a plurality of sectors, each of the sectors including a predetermined number of the

nonvolatile memory cells and serving as a basic unit for accessing the nonvolatile memory cell, wherein

the first digit line is disposed in a first sector while the second digit line is disposed in a second sector.

6. A nonvolatile semiconductor memory device as claimed in claim 5, wherein the first sector and the second sector are disposed adjoining each other.

7. A nonvolatile semiconductor memory device as claimed in claim 5, wherein the first digit line and the second digit line have equivalent physical parameters surrounding the digit line.

8. A nonvolatile semiconductor memory device having a plurality of local digit lines to which a plurality of nonvolatile memory cells are connected and a global digit line provided for each predetermined number of the local digit lines and to which the local digit line is selectively connected, wherein

upon reading memory cell information, the global digit lines include:

a first global digit line connected to a first local digit line to which the selected nonvolatile memory cell is connected; and

a second global digit line adjacent the first global digit line, to which the selected nonvolatile memory cell is not connected, while the memory cell information is read out with the first and second global digit lines as a pair.

9. A nonvolatile semiconductor memory device as claimed in claim 8, wherein the second global digit line is connected to a second local digit line to which only the non-selected nonvolatile memory cells are connected.

10. A nonvolatile semiconductor memory device as claimed in claim 9, wherein the first local digit line and the second local digit line adjoin each other.

11. A nonvolatile semiconductor memory device as claimed in claim 9, wherein the first local digit line and the second local digit line have equivalent physical parameters surrounding the first and second local digit lines.

12. A nonvolatile semiconductor memory device as claimed in claim 9, further comprising a plurality of sectors, each of the sectors including a predetermined number of the nonvolatile memory cells and serving as a basic unit for accessing the nonvolatile memory cell, wherein

a positional relationship of the first local digit line and the second local digit line is inverted every sector.

13. A nonvolatile semiconductor memory device as claimed in claim 9, further comprising a plurality of sectors, each of the sectors including a predetermined number of the nonvolatile memory cells and serving as a basic unit for accessing the nonvolatile memory cell, wherein

the first local digit line is disposed in a first sector while the second local digit line is disposed in a second sector.

14. A nonvolatile semiconductor memory device as claimed in claim 13, wherein the first sector and the second sector are disposed adjoining each other.

15. A nonvolatile semiconductor memory device as claimed in claim 13, wherein the first local digit line and the second local digit line have equivalent physical parameters surrounding the local digit line.

16. A nonvolatile semiconductor memory device as claimed in claim 12, wherein the positional relationship of the first global digit line and the second global digit line is inverted by each of the sector.

17. A nonvolatile semiconductor memory device as claimed in claim 13, wherein a positional relationship of the first global digit line and the second global digit line is inverted every sector.

18. A nonvolatile semiconductor memory device as claimed in claim 1, wherein a minimum unit of redundant configuration for recovery of a defect is comprised of the first and second digit lines making a pair.

19. A nonvolatile semiconductor memory device as claimed in claim 8, wherein a minimum unit of redundant configuration for recovery of a defect is comprised of the first and second global digit lines making a pair.

20. A nonvolatile semiconductor memory device

including a plurality of digit lines to which a plurality of nonvolatile memory cells are connected, wherein

the digit lines include a first digit line to which a selected one of the nonvolatile memory cells is connected; and

a second digit line to which only non-selected nonvolatile memory cells are connected, the nonvolatile semiconductor memory device further comprising a selecting portion provided for every predetermined number of the digit lines and for, upon reading memory cell information, selecting both the first and second digit lines and, upon writing memory cell information, selecting only the first digit line.

21. A nonvolatile semiconductor memory device as claimed in claim 20, further comprising a data line connected selectively to the digit line, wherein the selecting portion includes a switching portion for, upon reading memory cell information, connecting the digit line to the data line by a first current driving power and, upon writing memory cell information, connecting the digit line to the data line by a second current driving power which is larger than the first current driving power.

22. A nonvolatile semiconductor memory device as claimed in claim 21, further comprising a data line connected selectively to the digit line, wherein the selecting portion includes a first path leading from the digit line to the data line upon reading memory cell information and a second path leading from the data line to the digit line upon writing memory cell information.

23. A nonvolatile semiconductor memory device as claimed in claim 22, wherein the switching portion comprising the first path is comprised of a low voltage resistance element, while the switching portion comprising the second path is comprised of a high voltage resistance element.

24. A nonvolatile semiconductor memory device as claimed in claim 22, further comprising:

a first control portion for turning on/off the switching portion comprising the first path; and

a second control portion for turning on/off the switching portion comprising the second path, wherein

the first control portion is comprised of a low voltage resistance element while the second control portion is comprised of a high voltage resistance element.

25. A nonvolatile semiconductor memory device as claimed in claim 22, wherein the second path is so constructed as to include the first path.

26. A nonvolatile semiconductor memory device as claimed in claim 21, further comprising first and second switching portions for, upon reading memory cell information, connecting the first and second digit lines to respectively different the data lines and a third switching portion for, upon writing memory cell information, connecting the first digit line to the third data line.

27. A nonvolatile semiconductor memory device as claimed in claim 22, further comprising first and second

switching portions for, upon reading memory cell information, connecting the first and second digit lines to respectively different the data lines and a third switching portion for, upon writing memory cell information, connecting the first digit line to the third data line.

28. A nonvolatile semiconductor memory device as claimed in claim 20, further comprising a plurality of local digit lines to which a plurality of nonvolatile memory cells are connected and a global digit line provided for each predetermined number of the local digit lines and to which the local digit line is selectively connected, wherein

the digit line is the global digit line.

29. A nonvolatile semiconductor memory device having a plurality of digit lines to which a plurality of nonvolatile memory cells are connected and a data line connected selectively to the digit line, the nonvolatile semiconductor memory device further comprising:

a first data line to which the selected nonvolatile memory cell is connected through a first digit line;

a second data line to which only the non-selected nonvolatile memory cells are connected through a second digit line;

a first loading portion connected to the first data line; and

a second loading portion having a structure equivalent to that of the first loading portion, connected to the second data line and for supplying a reference current to a current flowing through the first data line based on the memory cell

information, wherein the memory cell information is read out with the first and second data lines as a pair.

30. A nonvolatile semiconductor memory device as claimed in claim 29, wherein the first and second loading portions have a load equivalent to a load existing on a path leading from the nonvolatile memory cell to the first and second loading portions.

31. A nonvolatile semiconductor memory device as claimed in claim 29, wherein the first and second loading portions have first and second reference cells equivalent to the nonvolatile memory cell.

32. A nonvolatile semiconductor memory device as claimed in claim 29, further comprising a regulating portion containing a third reference cell equivalent to the nonvolatile memory cell, for generating a reference current with respect to a current based on the memory cell information and outputting a regulation voltage corresponding to the reference current, wherein the first and second loading portions have first and second load portions in which a current value is controlled by the regulation voltage.

33. A nonvolatile semiconductor memory device as claimed in claim 31, wherein the first and second reference cells are disposed in a region different from an arrangement region of the nonvolatile memory cell in which the memory cell information is stored.

34. A nonvolatile semiconductor memory device as claimed in claim 31, further comprising first and second selecting switches for connecting the first and second reference cells to a reference potential, wherein any one of the first selecting switch and the second selecting switch is selectively turned on.

35. A nonvolatile semiconductor memory device as claimed in claim 32, wherein the third reference cell is disposed in a region different from an arrangement region of the nonvolatile memory cell in which the memory cell information is stored.

36. A nonvolatile semiconductor memory device as claimed in claim 32, further comprising first and second selecting switches for connecting the first and second load portions to a reference potential, wherein any one of the first selecting switch and the second selecting switch is selectively turned on.

37. A nonvolatile semiconductor memory device as claimed in claim 32, wherein the regulating portion includes a reference current generating portion containing the third reference cell, and a regulation voltage generating portion containing a third load portion equivalent to the first and second load portions.

38. A nonvolatile semiconductor memory device as claimed in claim 37, wherein the regulating portion includes a current mirror portion for mirroring a reference current

generated by the reference current generating portion to the regulation voltage generating portion, and a feedback portion for controlling the third load portion so as to supply the mirrored reference current to the regulation voltage generating portion.

39. A nonvolatile semiconductor memory device as claimed in claim 38, wherein the feedback portion outputs the regulation voltage.

40. A nonvolatile semiconductor memory device as claimed in claim 29, further comprising a plurality of local digit lines to which a plurality of nonvolatile memory cells are connected and a global digit line provided for each predetermined number of the local digit lines and to which the local digit line is selectively connected, wherein

the digit line is the global digit line.

41. A nonvolatile semiconductor memory device having a plurality of digit lines to which a plurality of nonvolatile memory cells are connected and a data line connected selectively to the digit line, the nonvolatile semiconductor memory device further comprising:

a first data line to which the selected nonvolatile memory cell is connected through the digit line and through which a current based on memory cell information flows;

a second data line through which a reference current flows; and

a current comparing portion to which the first and second data lines are connected and which compares a current based

on the memory cell information with the reference current, wherein

the current comparing portion includes a current load portion having a current mirror structure and a connection changing portion for changing a connection between the first and second data lines and the current load portion.

42. A nonvolatile semiconductor memory device as claimed in claim 41, wherein the connection changing portion is so controlled that the second data line is connected to a reference side in the current mirror structure of the current load portion.

43. A nonvolatile semiconductor memory device as claimed in claim 41, wherein the connection changing portion includes a voltage dividing portion for restricting a voltage applied to the current load portion side irrespective of a voltage of the first and second data lines.

44. A nonvolatile semiconductor memory device having a plurality of digit lines to which a plurality of nonvolatile memory cells are connected and a data line connected selectively to the digit line, the nonvolatile semiconductor memory device further comprising:

a first data line to which the selected nonvolatile memory cell is connected through the digit line and through which a current based on memory cell information flows;

a second data line through which a reference current flows; and

a current comparing portion to which the first and second

data lines are connected and which compares a current based on the memory cell information with the reference current, wherein

the current comparing portion includes a current load portion for supplying a current equivalent to the reference current to the first and second data lines.

45. A nonvolatile semiconductor memory device as claimed in claim 44, further comprising a voltage dividing portion for restricting a voltage applied to the current load portion side irrespective of a voltage of the first and second data lines, the voltage dividing portion being provided between the first and second data lines and the current load portion.

46. A nonvolatile semiconductor memory device as claimed in claim 41, further comprising a bias portion for restricting a voltage applied to the first and second data lines side irrespective of a voltage outputted from the current load portion.

47. A nonvolatile semiconductor memory device as claimed in claim 41, further comprising a plurality of local digit lines to which a plurality of nonvolatile memory cells are connected and a global digit line provided for each predetermined number of the local digit lines and to which the local digit line is selectively connected, wherein

the digit line is the global digit line.